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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,200	12/30/2003	Kyung Hee Koh	PIA31221/DBE/US	3418

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/751,200	KOH, KYUNG HEE
	Examiner	Art Unit
	Chuong A. Luu	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/13/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 5-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 5-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-2 and 5-12 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 1-2 and 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mukerji et al. (U.S. 6,300,679 B1) in view of Crafts et al. (U.S. 5,492,235) and further in view of Moon et al. (U.S. 2002/0164838 A1).

Mukerji discloses a semiconductor component with

Respect to claims:

(1) –a- connecting connection terminals (127) of a tape (120) of a conductive adhesive film, which a circuit is patterned to bond pads of the chip by applying an adhesive on the tape;

-b- applying an adhesive (303) an upper surface of the chip folding the tape and attaching the folded tape to the upper surface (343) of the chip (341);

-c- forming a plurality of ball terminals (201) on a lower surface of the tape (120), the ball terminals (201) being electrically connected to the connection terminals of the tape (127);

-d- manufacturing a plurality of individual chip scale packages by repeating the steps –a- to –c- (see column 4, lines 54-67. Figure 5);

-e- laminating the individual chip scale packages, wherein the ball terminals of an upper individual chip scale package is electrically connected to the circuit which covers lower individual chip scale package (see column 4, lines 54-67. Figure 5);

(2) further comprising the step of mounting the ball terminals of the lowest one of the individual chip scale packages on a patterned circuit (see Figure 4);

(3) wherein, in the step –a-, the chip is attached tape applying a conductive adhesive on the tape (see Figure 3);

(5) wherein, in the step the step –b-, the tape (120) is attached to the chip (341) applying a conductive adhesive (303) to the upper surface of the chip (341) (see Figure 4);

(6) further comprising the step of providing an uppermost chip scale package on top of the laminated chip scale packages of step (e), wherein the tape covers only a lower surface the uppermost one of the individual chip scale packages (see Figure 4);

(7) wherein the step of providing an uppermost chip scale package comprises connecting connection terminals of a further tape of a further anisotropic conductive

adhesive film on which a further circuit is patterned to bond pads of a further chip by applying a second adhesive on the tape, and forming a further plurality of ball terminals on a lower surface of the further tape, the further plurality of ball terminals being electrically connected to the connection terminals of the further tape (see Figure 4);

(8) wherein the second adhesive comprises a third anisotropic conductive adhesive (see Figure 4);

(10) comprising the step of patterning the circuit on the tape (see Figure 4);

(11) wherein, in step (b), the adhesive comprises a thermal conductive adhesive (see Figure 4);

(12) wherein the patterned circuit comprises a printed circuit board (see Figure 4).

Mukerji teaches the above outlined features except for using a first C4 process and on an outer surface of the tape. However, Crafts discloses a semiconductor device by using a first C4 process **(9)...** uses a first C4 process; **(9)** wherein the step of connecting the connection terminals of the further tape uses a second C4 process; (see column 3, lines 48-60). Furthermore, Moon discloses an integrated circuit with **(9)...** on an outer surface of the tape (see Figure 2A). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the packaged device of Mukerji and Crafts (accordance with the teaching of Moon). Doing so would facilitate the manufacture of the semiconductor package device and increase the bonding between the chip and the pads and speed of the semiconductor device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
December 15, 2005